Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at said input a direction of change in voltage of said input signal; and

introducing a current to said parasitic capacitance to prevent ~~compensate for current of said input signal charging~~ said parasitic capacitance from drawing current from said input signal responsive to detection of a positive edge of said input signal.

2. (Previously presented) The method of claim 1, wherein said signal is applied to the input of said circuit.

3. (Previously presented) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at the input of said circuit a direction of change in voltage of said input signal; and

preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal.

4. (Withdrawn) A method for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising the steps of:

detecting a change in voltage of said input signal; and

changing an impedance of a parallel termination circuit that is in parallel with said parasitic capacitance to reduce distortion of said input signal.

5. (Previously presented) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance between said input and ground, comprising:

a detection circuit coupled to said input for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled between said detection circuit and said input for compensating for current from said input signal diverted to said parasitic capacitance due to a positive edge of said input signal.

6. (Original) The apparatus of claim 5, wherein said detection circuit includes a capacitance.

7. (Canceled)

8. (Previously presented) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance between said input and ground, comprising:

a detection circuit coupled to said input for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled between said detection circuit and said input for compensating for current from said parasitic capacitance to be added to said input signal due to a negative edge of said input signal.

9. (Original) The apparatus of claim 8, wherein said detection circuit includes a capacitance.

10. (Canceled)

11. (Withdrawn) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a detecting circuit for detecting a change in voltage of said input signal; and

a correction circuit for changing an impedance of a parallel termination circuit that is in parallel with said parasitic capacitance to reduce distortion of said input signal.

12. (Currently Amended) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at said input a direction in change in voltage of said input signal; and

introducing a current to said parasitic capacitance prevent ~~to compensate for~~ distortion of said input signal due to said parasitic capacitance responsive to detection of a positive edge of said input signal.

13. (Currently Amended) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting directly at said input a direction of change in voltage of said input signal; and

preventing introduction of a current from said parasitic capacitance into said input signal responsive to detection of a ~~positive~~ negative edge of said input signal.

14. (Withdrawn) Apparatus for reducing distortion of an input signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance at said input, comprising:

a first circuit element for selectively providing current to said parasitic capacitance;

a second circuit element for selectively preventing discharge of said parasitic capacitance; and

a control circuit monitoring said input signal for respectively turning on said first circuit element and turning off said second circuit element when a positive going edge of said input signal is detected and for turning off said first circuit element and turning on said second circuit element when a negative going edge of said input signal is detected.

15. (Withdrawn) The apparatus of claim 14 wherein said first and second circuit elements have a common terminal coupled to said parasitic capacitance.

16. (Withdrawn) Apparatus for reducing distortion of an input signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance at said input, comprising:

a first circuit element for selectively providing current to said parasitic capacitance;

a second circuit element for selectively preventing discharge of said parasitic capacitance; and

a control circuit monitoring said input signal for respectively turning on said first circuit element and turning off said second circuit element when a positive going edge of second circuit element when a negative going edge of said input signal is detected;

said first and second circuit elements have a common terminal coupled to said parasitic capacitance;

said first and second circuit elements being transistors.

17. (Withdrawn) The apparatus of claim 16 wherein one of said transistors is a PMOS transistor and another one of said transistors is an NMOS transistor.

18. (Previously presented) The method of claim 1 wherein, said introducing step includes introducing the current to said input.

19. (Canceled)

20. (Canceled)

21. (Withdrawn) The apparatus of claim 11 wherein said parasitic capacitance appears between said input and ground.

22. (Canceled)

23. (Canceled)

24. (Withdrawn) The apparatus of claim 14 wherein said parasitic capacitance appears between said input and ground.

25. (Previously added) The apparatus of claim 6 wherein the capacitance of the detection circuit has one terminal directly connected to one terminal of the parasitic capacitance.

26. – 27. (Canceled)

28. (Previously presented) The apparatus of claim 5 wherein said circuit has an output, said detection circuit being isolated from said output.

29. (Previously presented) The apparatus of claim 8 wherein said circuit has an output, said detection circuit being isolated from said output.

30. (Currently amended) The apparatus of claim 5 wherein said detection circuit is independent of said ~~first mentioned~~ circuit operating at high frequency.

31. (Currently amended) The apparatus of claim 8 wherein said detection circuit is independent of said ~~first mentioned~~ circuit operating at high frequency.